TAMS 82622 PCI GPIO Card for Linux

Installation & Operation Instructions

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General Information

Overview of the TAMS 82622 GPIO Interface

This guide explains how to install and configure the TAMS 82622 GPIO (General Purpose Input Output) interface.

The TAMS GPIO card has a rotary DIP switch on the upper edge to set the unique identifier for the card. This is the only switch that needs to be set prior to installing the card. All other configuration is done in software.

Since the configuration of the GPIO interface (aside from setting the unique card identifier) is done in software, rather than using DIP-switches or jumpers, this guide also provides an explanation of the configuration process as it relates to SICL. A detailed description of the TAMS GPIO's functionality is included to aid in this configuration process.

There are two basic modes for the data ports in the TAMS GPIO interface. The TAMS GPIO is by default configured like the HP 98622 GPIO interface, which is called *Compatibility Mode*. Alternately, the TAMS 82622 can be configured with a bi-directional data port and auxiliary control lines, which is called *Enhanced Mode* and is supported by HP 2074/5 and all TAMS GPIO cards.

Installing the Interface

This section explains how to install the TAMS GPIO interface in the computer. To complete the installation:

1. Make sure the computer is shut down properly, the power is turned off, and the power cord is unplugged.
2. Refer to the Owner's Guide of your computer for instructions on opening your computer and installing PCI boards.
3. The rotary DIP switch on the upper edge of the TAMS 82622 card should be set to the PCI slot number the card is going to reside in. If you have multiple TAMS 82622 cards installed in a single machine, it is important that the rotary DIP switches each be set to a unique number, which is guaranteed if you set the switch to the slot number. (Be sure to note the position of the rotary DIP switch, as you will need to know this when you configure the card.)
4. Install the GPIO interface in the PC by plugging the card into the PCI slot.
5. Follow the instructions being careful to handle the TAMS 82622 board only by its metal bracket. Avoid contact with the edge connector. After the board has been plugged in and the retaining screw installed the computer should be reassembled.
6. Prepare and install the GPIO interface cable.

Driver Installation

Note: Driver installation assumes basic knowledge about software installation procedures specific to the platform. Refer to your platform specific operating system documentation or contact your system administrator.

To install the t82622 driver it is not necessary for the TAMS 82622 interface card(s) to be present in the system.

Note: You must have root permission to install the software. Installation of the TAMS GPIO driver (T82622) also requires that the TAMS I/O Libraries (T82091) are already installed.

1. Insert the installation media into the drive and wait for the busy light to remain off.

2. If your system does not automount the CD-ROM, mount the CD-ROM. To do this you will need to know the device file for your CD-ROM drive and the directory where you wish to mount it. These can vary depending upon your hardware and Linux distribution.

   On **Red Hat Enterprise Linux Workstation 3**, this is usually accomplished with

   ```
   /bin/mount /dev/cdrom /mnt/cdrom
   ```

   On later versions of **Red Hat Enterprise Linux Workstation**, this is usually accomplished with

   ```
   /bin/mount /dev/cdrom /media/cdrecorder
   ```

3. Install the software. There are two ways in which you may do this.

   If you wish to install the current version of the TAMS I/O Libraries and all related drivers, including the one for the 82622, simply run the INSTALL program from the CD-ROM.

   ```
   /media/cdrecorder/INSTALL
   ```

The exact location will vary depending on where you mounted the CD-ROM in Step 2.

If you already have the TAMS I/O Libraries installed, you may install this driver manually.

```
cd /media/cdrecorder/RHEL4u3.i686
rpm -Uvh T82622-2.0-RHEL4u3.i686.rpm
```

The directory and filename will vary depending on the operating system distribution, processor architecture, and driver revision. Some directories have a 'whichrpm.sh' script in them, which should be used to determine the RPM architecture. In these cases, installation will look more like this. (Note the use of backquotes rather than single quotes.)

```
cd /media/cdrecorder/RH9RHEL3.i686
rpm -Uvh T82622-2.0-RH9RHEL3.`./whichrpm.sh`.rpm
```

4. The T82622 RPM will automatically load the t82622 kernel module and create the necessary device files. Each time you start up your computer after this, the t82622 kernel module will be loaded and related device files will be created.

5. Once the installation is complete, unmount the CD.

```
cd /
/bin/umount /dev/cdrom
```

6. Once the CD is unmounted, remove the media from the drive and store it in a safe place.

In general, the installation procedure places the files in the necessary directories by default. Appendix B is a reference for the Linux systems administrator, who might wish to know where these files are placed.

You will still need to configure the new TAMS GPIO card as a SICL interface card, as covered in the next section.

Interface Configuration

After installation of the driver software and loading of the t82622 kernel module (handled automatically by the RPM package), the SICL configuration file `/etc/opt/sicl/hwconfig.cf` needs to be edited to reflect the new interface card. The version of SICL you are using includes the `/opt/sicl/bin/iosetup` program, this can be used in place of manually editing the `hwconfig.cf` file. You will still want to refer to this section for a description of the fields.)

After configuration, the system does NOT need to be rebooted, nor does the driver module need to be reloaded. However, the SICL iclear function should be used after making changes to ensure that the configuration changes have taken effect. See the man page on iclear (1).

For further configuration information, see the “Installing and Configuring the I/O Libraries” chapter of the *I/O Libraries Installation and Configuration Guide for Linux*.

For each TAMS 82622 card that you want to configure in your system, you need to add a line to the `hwconfig.cf` file. While most users do not need to see or use this file directly, having used iosetup to make configuration changes, the fields and their respective meanings are important to know to properly use the GPIO card.

The content of each line is as follows:

<lu> <name> t82622 <location> <res> <polarity> <mode> <read_clk> <delay>

The fields are defined as:

Logical Unit (lu) The SICL Logical Unit number for this interface. This number must be unique for the SICL interfaces currently configured on this machine. A good choice for a logical unit number would be 12.

Symbolic Name (name) The unique SICL symbolic name. A good choice would be “`gpio`”.

Location The unique ID specified by the rotary DIP switch on the TAMS 82622 being configured. This value is in the range 0-9

Reserved (res) Unused on the 82622. Must always be “0”.

Polarity The logic polarity of various interface lines. Each bit controls the polarity of one function:

0b<Pullup><Data Out><Data In><PSTS><PFLG><PCTL>.

PCTL:
0 = "Low = Set"
1 = "High = Set"
PFLG:
0 = "Low = Ready"
1 = "High = Ready"
PSTS:
0 = "Low = Not Ok"
1 = "High = Not Ok"
Data In/Data Out:
0 = "Low = 1"
1 = "High = 1"
Pullup:
0=do NOT enable pullup resistors
1=DO enable them

Mode A 2-digit hexidecimal number that configures handshake and data port mode. The most significant digit configures the data port.

HP 98622 compatibility mode:
0 = No DOUT clear at reset
1 = Clear DOUT at reset
Enhanced (bi-directional DINs) data port:
2 = No DOUT clear at reset
3 = Clear DOUT at reset

The least significant digit selects the PFLG/PCTL handshake mode.

0 = Full handshake
1 = Pulse handshake
2 = Async-Write/Pulse-Read handshake

For example, 0x10 specifies compatibility mode with DOUT cleared on reset and full handshaking.

Read Clock (read_clk) Determines when data input registers are latched. The first hex digit is for the upper (most significant) byte. Second hex digit is for the lower byte. Valid values for each digit are:

0 = when register is read (approx 500 ns after the handshake is initiated)
1 = when PFLG transitions to 'busy'
2 = when PFLG transitions to 'ready'

Delay The delay (settling time) from data output to PCTL set:

0 = 200 nanoseconds
1 = 400 nanoseconds
2 = 700 nanoseconds
3 = 1.2 microseconds
4 = 2 microseconds
5 = 5 microseconds
6 = 10 microseconds
7 = 50 microseconds

The t82622 driver provides an alternative delay configuration method. The delay may be expressed in nanoseconds or in microseconds in hwconfig.cf. If the delay is expressed in nanoseconds the decimal value representing that delay should be suffixed with “ns”. If the delay is expressed in microseconds the decimal value representing delay should be suffixed with “us”. A decimal point is allowed. The minimum delay is 30ns and maximum delay is 61.41us. Examples: 150ns, 2500ns (same as 2.5us), 1.15us, 50us.

When Configuration Changes take Effect

Configuration changes take effect when the first process does the first iopen() on the GPIO card. To ensure this happens, make sure no processes are running that use the I/O libraries when the configuration of the card is changed.

It is not necessary to reboot or to reload the driver kernel module for changes to take effect.

It is safest to perform an `iclear` on the interface after modifying its configuration to guarantee that it is in a known state.

Related Software Documentation

Standard Instrument Control Library for Linux

To configure the TAMS GPIO interface for the Standard Instrument Control Library (SICL) for Linux, see the “Installing and Configuring the I/O Libraries” chapter of the *I/O Libraries Installation and Configuration Guide for Linux*.

To develop SICL I/O applications for the TAMS card on Linux, see the “Using GPIO with SICL” chapter of the *SICL User’s Guide*. SICL functions, including those that are GPIO specific, are fully defined in the *SICL User’s Guide*. The TAMS card also provides functionality enhancements.

BASIC for Linux

The TAMS GPIO interface is supported on version 11.0 and later of TAMS BASIC for Linux.

When the GPIO interface has been configured for SICL, it is also ready to be used from within BASIC for Linux. BASIC users will need to know the SICL Logical Unit Number that has been assigned to the interface during configuration, as this will correspond to the Select Code used to identify the interface in their BASIC programs.

More information for the use of the GPIO interface is found on the TAMS BASIC Documentation CD. Relevant sections are the “Linux Highlights” section of the *BASIC Language Reference*, and the GPIO chapter of the *BASIC Interface Reference* on the CD.

Additional GPIO Documentation Online

Technical articles and other additional GPIO documentation can be found on the TAMS web site: http://www.tamsinc.com/support/

Technical Information

This section provides a detailed, functional description of the TAMS 82622 GPIO interface. You will need to understand this information in order to set the appropriate configuration values. This information should also be helpful when you are preparing and installing the GPIO cable.

After you have read this section and decided how you want to configure the TAMS 82622 card, refer to your software documentation to configure your I/O application software for the TAMS 82622 card. (See the “Related Software Documentation” section of this guide.)

This section contains the following :

- Connector Pinouts
- Data Lines
- Peripheral Information Lines:
  - Peripheral Control and Peripheral Flag Handshake Lines (PCTL and PFLG)
  - Input/Output Direction Control Line (I/O)
  - Peripheral Status Line (PSTS)
  - Peripheral Reset Line (P_RESET)
  - External Interrupt Request Line (EIR)
  - Control Output Lines (CTL0 and CTL1)
  - Status Input Lines (STI0 and STI1)
- Direct Memory Access (DMA)

Appendix A: General Specifications

PCI implementation: revision 2.3, 32 bit, 33 Mhz

Card voltage requirements (PCI)

+5 volts, +-5%, at 0.45A max (plus current sourced from pin 50)

(changing pullup resistors may increase max current draw on +5)

+3.3 volts, +- 10%, at 1 ma max

PCI signaling voltage:

3.3 or 5 volts, universal keying

Dimensions:

4.75 by 4.00 inches, exclusive of PCI bracket

Weight:

4.0 oz.

Operating environment:

0 to 40 degrees C

10 to 90% RH, non-condensing

Storage environment:

-20 to 70 degrees C

5 to 95% RH

Maximum Current Sourced by Card:

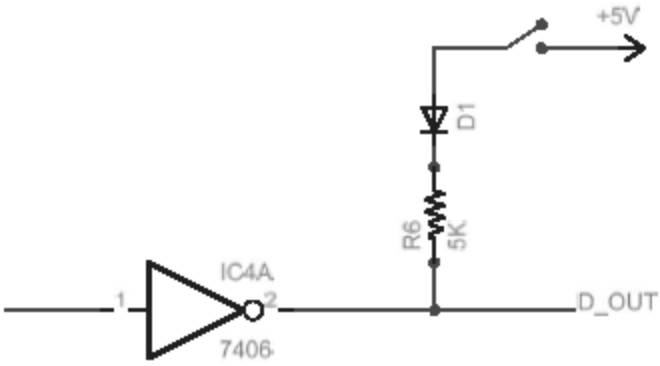
.75 amps from pin 50 of I/O connector.

Appendix B: Output Circuitry

A typical output line from the card is shown below. The driver is open-collector TTL, with 40 ma pulldown capability and 30 volt max voltage rating. As a convenience, there are 5K pullup resistors to +5 volts provided. These can be switched on and off under software control. They are also socketed, to allow easy removal if the external circuitry requires. If they are re-inserted, be careful to observe the polarity markings.

The blocking diodes are rated at greater than 30 volts, so the on-board resistors can safely be left installed if the outputs are pulled up to greater than 5 volts by external circuitry. Care must be taken to insure that the voltage on the outputs does not exceed 30 volts due to transmission line effects from a cable, or inductive kickback from switched loads.

The pullup resistors are 12 pin SIP style, installed in J1-J4. If driving long cables, signal quality constraints may require lower value resistors to provide adequate current sourcing. Never use less than 120 ohms, due to current constraints of the drivers. One suitable source for 120 ohm resistor packs is Bournes, PN 4612X-102-121LF, four per card. These are 'isolated', not 'bussed' or 'common'. See the GPIO Support section of the TAMS website for information on driving long cables.



Example circuitry for output lines.

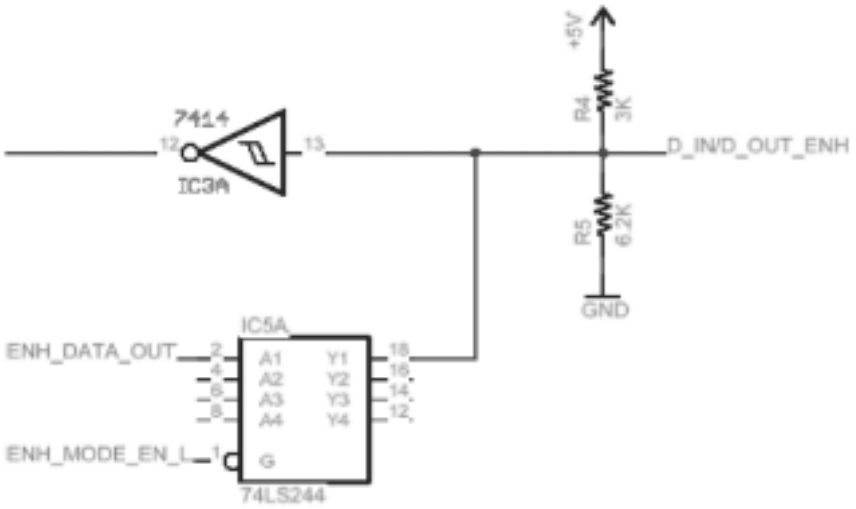
(DOUT_x, PCTL, CTL_0, CTL_1, I/O, P_RESET)

Appendix C: Input Circuitry

There are two types of inputs to the card, the DIN lines, and the control lines. The DIN lines are input-only in compatibility mode, and bi-directional in enhanced mode. The input control lines are always input-only. The diagram below shows typical circuitry for the DIN lines, the control lines are similar but do not include the 74LS244 type of driver.

As inputs, the lines are biased at approximately 3.3 volts to provide a high level. Schmitt trigger logic is used to help reduce problems from slow transitions, or noisy environments. When these lines are driven as outputs (only during enhanced mode), they can source 15 ma and sink 24 ma. Since these are implemented with TTL logic, the input voltage range is 0-5 volts.

If these inputs are receiving signals from a long cable, note that the high impedance of the circuitry provides no significant termination of the lines. It may be necessary to provide termination between the cable and the 82622 card in order to achieve good signal integrity. See the GPIO Support section of the TAMS website for more information on using long cables.

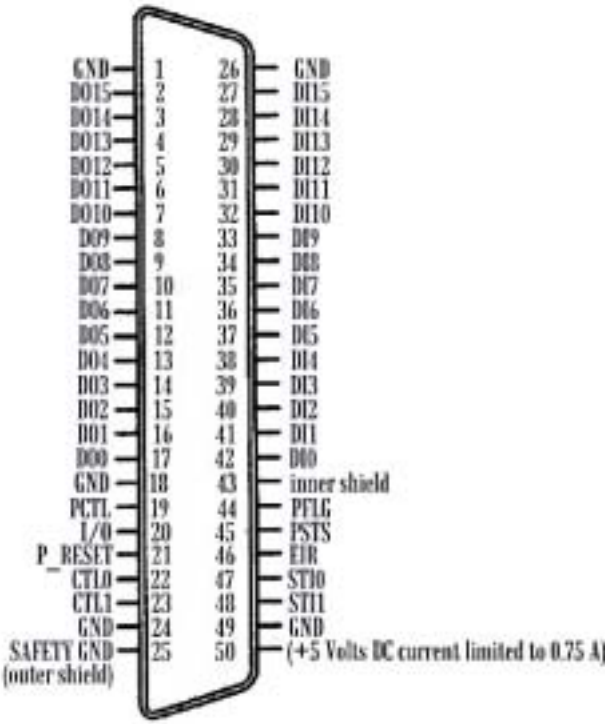


Typical input line/enhanced line circuitry (DIN_x).

Input control lines similar, but without the 74LS244.
(PFLG, PSTS, ST_0, ST_1, EIR)

Appendix D: Connector Pinouts

The following figure shows you the Pinouts on the TAMS 82622 GPIO interface connector.



TAMS 82622 GPIO Connector Pinouts

Appendix E: Wiring

Data Lines

There are 32 data lines on the TAMS GPIO: 16 designated as data input, and 16 designated as data output. Color codes are provided for the TAMS 622-001 GPIO cable and the HP 5061-4209 GPIO cable.

Label	Line(s)
DI0 through DI15	Data Input
DO0 through DO15	Data Output
PCTL and PFLG	Peripheral Control and Peripheral Flag handshake
I/O	Input/Output direction control
PSTS	Peripheral Status
P_RESET	Peripheral Reset
EIR	External Interrupt Request
CTL0 and CTL1	Control Output
STI0 and STI1	Status Input
PIN 50	+5 Volts DC current limited to 0.75 A

Data Input Lines

The 16 data input lines are labeled DI0 through DI15. The following table lists the connector pin numbers and cable wire color codes for the data input lines.

Data Input Lines

Label	Pin No.	622-001	5061-4209
DI0	42	White on Grey	Black
DI1	41	Brown on Blue	Brown
DI2	40	White on Violet	Red
DI3	39	White on Blue	Orange
DI4	38	White on Green	Yellow
DI5	37	White on Yellow	Green
DI6	36	White on Orange	Blue
DI7	35	White on Pink	Violet
DI8	34	Brown on Green	White/Brown/Red
DI9	33	Brown on Yellow	White/Brown/Orange
DI10	32	Brown on Orange	White/Brown/Yellow
DI11	31	Brown on Pink	White/Brown/Green
DI12	30	Tan on Grey	White/Red/Orange
DI13	29	Tan on Violet	White/Red/Yellow
DI14	28	Tan on Blue	White/Red/Green
DI15	27	Tan on Green	White/Red/Blue

Data Output Lines

The 16 data output lines are labeled DO0 through DO15. The following table lists the connector pin numbers and wire color codes for the data output lines.

Data Output Lines

Label	Pin No.	622-001	5061-4209
DO0	17	Grey on White	White/Black
DO1	16	Blue on Brown	White/Brown
DO2	15	Violet on White	White/Red
DO3	14	Blue on White	White/Orange
DO4	13	Green on White	White/Yellow
DO5	12	Yellow on White	White/Green
DO6	11	Orange on White	White/Blue
DO7	10	Pink on White	White/Violet
DO8	9	Green on Brown	White/Orange/Yellow
DO9	8	Yellow on Brown	White/Orange/Green
DO10	7	Orange on Brown	White/Orange/Blue
DO11	6	Pink on Brown	White/Orange/Violet
DO12	5	Grey on Tan	White/Yellow/Green
DO13	4	Violet on Tan	White/Yellow/Blue
DO14	3	Blue on Tan	White/Yellow/Violet
DO15	2	Green on Tan	White/Yellow/Gray

Peripheral Information Lines

The following table lists the connector pin numbers and wire color codes for the peripheral information lines.

Peripheral Information Lines

Label	Pin No.	622-001	5061-4209
GRD	1	Yellow on Tan	
GRD	18	Violet on Brown	
PCTL	19	Tan on White	White/Grey
I/O	20	Grey on Brown	White/Black/Brown
P_RESET	21	Orange on Pink	White/Black/Red
CTL0	22	Brown on Tan	White/Red/Violet
CTL1	23	Pink on Tan	White/Red/Grey
GRD	24	Brown on White	
Safety GRD	25	Orange on Tan	
GRD	26	Tan on Yellow	
Safety GRD	42	Brown on Violet	
PFLG	44	White on Tan	Grey
PSTS	45	Brown on Grey	White/Black/Grey
EIR	46	Pink on Orange	White/Brown/Grey
STI0	47	Tan on Brown	White/Brown/Blue
STI1	48	Tan on Pink	White/Brown/Violet
GRD	49	White on Brown	
+5 (fused)	50	Tan on Orange	

Appendix F: File Locations

The installation procedure places files in the following directories :

File	Location	Description
t82622.so	/opt/sicl/lib	SICL shared Tulip library
t82622.o t82622.ko	/lib/modules/<kernel version> kernel/drivers/char	kernel driver module
t82622	/etc/init.d	stop/start script for (un)loading the kernel module and (un)creating the device files
s95t82622 k05t82622	/etc/rc[345].d	link to /etc/init.d/t82622
t82622.n	/dev	special device file for card with ID n

Appendix G: TAMS GPIO SICL Extensions

All of the TAMS GPIO SICL extension functions are implemented by using the header file tamsgpio.h and the standard SICL functions igpioctrl and igpiostat.

These two functions are described below:

IGPIOCTRL

Supported sessions: . . . . . **interface**
Affected by functions: . . . . . **ilock, itimeout**

C Syntax

```
#include <sicl.h>
#include <tamsgpio.h>

int igpioctrl (id, request, setting);

INST id;
int request;
unsigned long setting;
```

IGPIOSTAT

Supported sessions: . . . . . **interface**

C Syntax

```
#include <sicl.h>
#include <tamsgpio.h>

int igpiostat (id, request, result);

INST id;
int  request;
unsigned  long  result;
```

The following are all of the TAMS 82622 SICL extensions and some examples of how to use them.

TAMS 82622 PCTL delay

The TAMS 82622 PCTL delay function provides an **extended PCTL delay control** that was not available prior to the 81622. Besides the standard 0-7 values for delay used with HP cards, the delay of the TAMS 82622 can be set directly in nanoseconds.

Examples:

Setting the PCTL delay to 50000ns

```
igpioctrl(id, I_GPIO_PCTL_DELAY, 7)

or

igpioctrl(id, T_GPIO_DLY_TM, 50000)
```

Reading the PCTL delay in nanoseconds

```
igpiostat(id, T_GPIO_DLY_TM, &dtm)
```

Legal values are 30 to 61410 ns. The value configured in 'iosetup' is used, unless overwritten by an igpioctrl call.

TAMS 82622 Filtering

This feature allows filtering of DIN[0..15], PCTL, STI0, STI1 and EIR lines for glitch rejection.

T_GPIO_FLT_TM sets the filtering time in nanoseconds of the input filters. No individual lines may be controlled. Since the PCTL handshake is filtered to the same extent as the data lines, the setup time during a read does not change when filtering is increased.

Examples:

Using **T_GPIO_FLT_TM**

Set filtering to 1 microsecond

```
igpioctrl(id, T_GPIO_FLT_TM, 1000)
```

Read the time set for filtering in nanoseconds

```
igpiostat(id, T_GPIO_FLT_TM, &ftm)
```

Legal values are 0 to 1860 ns, where 0 ns provides no filtering. This is the default.

TAMS 82622 Polarity

This function allows for individual polarity setting for **DIN, STI0, STI1, and EIR.** The polarity of nineteen lines (DIN[0..15], STI[0..1] and EIR) can be controlled independently.

When a bit in the polarity bitmask is set to 0, that line is active low polarity; when set to 1, that line is active high polarity.

To maintain maximum compatibility with the HP GPIO, the following rules apply:

- For STI and EIR lines, if their polarity is set to 0, their behavior is fully compatible with standard GPIO. If set to 1, polarity is reversed for these lines.
- For DIN lines, 82622 extensions allow the user to set the polarity for each line independently. Setting the DIN polarity with standard GPIO SICL igpioctrl (**`id, I_GPIO_POLARITY, setting`**) is still supported and will cause the setting or clearing of all the DIN lines' polarity with a single parameter.

Examples:

Setting active high polarity for only DIN6 and EIR lines

igpioctrl(id, T_GPIO_POL, T_GPIO_DIN06 | T_GPIO_EIR)

Reading back the polarity setting

igpiostat(id, T_GPIO_POL, &pol);

TAMS 82622 Latching

This function allows latching the levels of the lines to be enabled in the three different groups (**DIN[0..15], STI0, STI1, and EIR lines)**. The time at which the latching occurs depends upon the polarity of the line being latched.

- If the polarity is set to 0, the latch will occur on a LO to HI logical transition.
- If the polarity is set to 1, the latch will occur on a HI to LO logical transition.

This function has three different request codes:

- **T_GPIO_LAT_EN** controls which group of lines are enabled for latching, DIN[0..15], STI0, STI1 and/or EIR.
- **T_GPIO_LAT_RD** lets you read the latched lines.
- **T_GPIO_LAT_CL** clears the latched lines.

Examples:

Enable T82622_DIN06 and T82622_EIR
igpioctrl (id, T_GPIO_LAT_EN, T_GPIO_DIN06 | T_GPIO_EIR)
Read what lines are enabled for latching
igpiostat(id, T_GPIO_LAT_EN, &len)
Read back what lines are latched
igpiostat(id, T_GPIO_LAT_RD, &lat)
Clear latched lines
igpioctrl(id, T_GPIO_LAT_CL, lat)

TAMS 82622 line interrupt

This function controls which lines can cause an interrupt**. Interrupts on level transitions on DIN[0..15], STI[0..1] and EIR lines** can be controlled individually. When the interrupt occurs depends upon the polarity:

- If the polarity is set to 0, the interrupt occurs on logical LO to HI transitions
- If the polarity is set to 1, the interrupt occurs on logical HI to LO transitions.

If one or more interrupts occur, the interrupt handler is called with the “reason” parameter equal to I_INTR_GPIO_T82622 and the “sec” parameter is the mask of the lines that caused the interrupt.

The mask is always a subset of the following:

T_GPIO_DIN | T_GPIO_STI | T_GPIO_EIR | T_GPIO_RDY

Examples:

Enabling DIN4 line to interrupt
igpioctrl(id, T_GPIO_INT_EN, T_GPIO_DIN04)
Checking what lines can interrupt
igpiostat(id, T_GPIO_INT_EN, &int)

TAMS 82622 Pull-up Resistors

T_GPIO_PUL controls if DOUT[0..15], CTL[0..1], PCTL, I/O, and PRESET lines are pulled up with 5K resistors to +5V. There is no control for individual lines. All lines are controlled at the same time. The SIP packs can be removed or changed by users.

Examples:

Turn all pull-ups ON

igpioctrl(id, T_GPIO_PUL, 1)

Check if pull-ups are on

igpiostat(id, T_GPIO_PUL, &pull)

Turn pull-ups OFF

igpioctrl(id, T_GPIO_PUL, 0)

TAMS 82622 Board ID

The 82622 is equipped with a rotary DIP switch. Its purpose is the identification of each GPIO board on a system with multiple GPIO cards.

The user must set the switch position to a unique value for each card on the system and then can read its value by using the request **T_GPIO_CID** to check which physical card is associated with a specific opened session.

Examples:

Get the switch value

igpiostat(id, T_GPIO_CID, &swID)

TAMS 82622 DOUT read

The **T_GPIO_DOUT** reads the value of the DOUT lines. The value read is not affected by the DOUT polarity.

Example:

Get the DOUT value

igpiostat(id, T_GPIO_DOUT, &dout)

TAMS 82622 Macros

The following is a table with all of the macro definitions passed to the TAMS 82622 SICL extension functions. Individual bits may be passed to select specific line(s).

TAMS 82622 SICL extension function defines

T_GPIO_DIN	0x0000FFFF	DIN[0..15] 16 bits
T_GPIO_DIN_L	0x000000FF	DIN[0..7] 8 bits
T_GPIO_DIN_U	0x0000FF00	DIN[8..15] 8 bits
T_GPIO_STI	0x00030000	STI[0..1] 2 bits
T_GPIO_EIR	0x00040000	EIR 1 bit
T_GPIO_RDY	0x00080000	RDY 1 bit
T_GPIO_MORE	0x00100000	used inside driver only
T_GPIO_ALL	0x000FFFFF	all of above 20 bits

Individual bits for DIN and STI

T_GPIO_DIN00	0x00000001
T_GPIO_DIN01	0x00000002
T_GPIO_DIN02	0x00000004
T_GPIO_DIN03	0x00000008
T_GPIO_DIN04	0x00000010
T_GPIO_DIN05	0x00000020
T_GPIO_DIN06	0x00000040
T_GPIO_DIN07	0x00000080
T_GPIO_DIN08	0x00000100
T_GPIO_DIN09	0x00000200
T_GPIO_DIN10	0x00000400
T_GPIO_DIN11	0x00000800
T_GPIO_DIN12	0x00001000
T_GPIO_DIN13	0x00002000
T_GPIO_DIN14	0x00004000
T_GPIO_DIN15	0x00008000
T_GPIO_STI0	0x00010000
T_GPIO_STI1	0x00020000

ONE YEAR LIMITED WARRANTY

Test & Measurement Systems, Inc. warrants to the purchaser that the Interface card will be free of all defects in material and/or workmanship for one year from the date of shipment to the customer.

In the event of malfunction or failure attributable directly to faulty material and/or workmanship, TAMS will at it's option, repair or replace the defective product or components, to whatever extent it shall deem necessary to restore the product or component, to proper operating condition. TAMS may at its option repair or replace, a defective unit with a new or refurbished unit.

The customer shall be solely responsible for the failure of any TAMS product, resulting from accident abuse, or misapplication of the product, and TAMS assumes no liability as a consequence of such events under the terms of this warranty.

While TAMS has made every effort to provide clear and accurate technical information about the application of this product, TAMS assumes no liability for any events arising out of the use of this technical information.

This Warranty gives you specific legal rights and you may also have other rights which vary from state to state, and from country to country.

This Warranty is in Lieu of all other express warranties which now or hereafter might otherwise arise with respect to this product. ANY AND ALL IMPLIED WARRANTIES OF MERCHANT ABILITY AND FITNESS FOR PARTICULAR USE, SHALL HAVE NO GREATER DURATION THAN THE PERIOD FOR THE EXPRESS WRITTEN WARRANTY APPLICABLE TO THIS PRODUCT AS SHOWN ABOVE, AND SHALL TERMINATE AUTOMATICALLY AT THE EXPIRATION OF SUCH PERIOD.

(Some states and countries do not allow limitations on how long an implied warranty lasts, so this limitation may not apply to you) No action shall be brought for breach of any implied or express warranty after one year subsequent to the expiration of the period of the express written warranty.

Incidental and consequential damages caused by malfunction, defect, or otherwise and with respect to breach of any express or implied warranty, are not the responsibility of TAMS, and to the extent permitted by law, are hereby excluded both for property and to the extent not unconscionable, for personal injury damage. (Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you.)

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